3750
10-BIT D/A CONVERTER
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3750 is a monolithic MOS/LSI ten bit digital to analog converter using P-channel enhancement mode MOS technology. The digital word can be entered serially or in parallel. If desired, the word is available in serial form through an output buffer in either an 8 or 10 bit format. The converter output data is available thru 10 single pole double throw (SPDT) MOS switches. The holding register retains the state of the previous digital input word and drives the output switches. Transfer gates are used to isolate the holding register from the input register while new data is being entered. The 'on' resistance of the MOS switches is weighted to provide the necessary accuracy and stability for a ten bit conversion.

FEATURES

- **8 AND 10 BIT DATA LENGTHS**
- **SERIAL AND PARALLEL OPERATION**
- **250 kHz SERIAL BIT RATE**
- **500 kHz PARALLEL WORD RATE**
- **250 Ω TYPICAL 'ON' RESISTANCE OF TWO MSB's**
- **500 Ω TYPICAL 'ON' RESISTANCE OF REMAINING EIGHT BITS**
- **110 mW POWER DISSIPATION**
- **ZERO AND FULL SCALE CALIBRATION LOGIC**

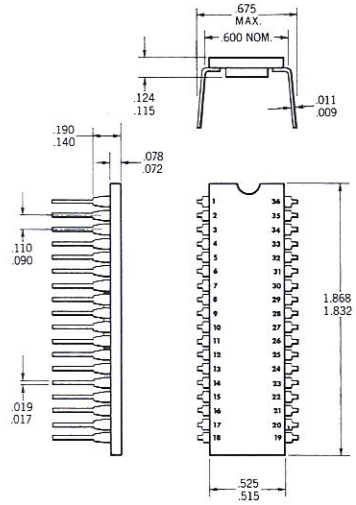
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Input Voltages	−30 to +0.3 Volts
Power Supply	−29 Volts
Storage Temperature	−55°C to +150°C
Operation Temperature	−55°C to +85°C

APPLICATIONS

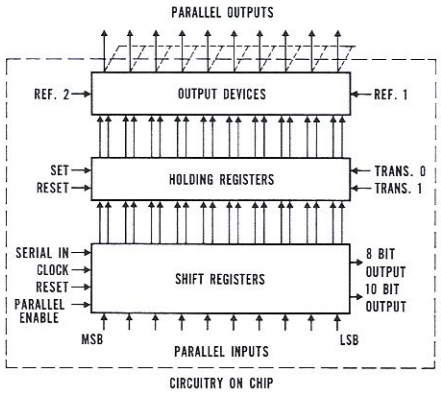
D/A Converters
- Telemetry
- Analog data plotters
- Industrial process control
- Servo systems

PHYSICAL DIMENSION
36 PIN
DUAL IN-LINE PACKAGE

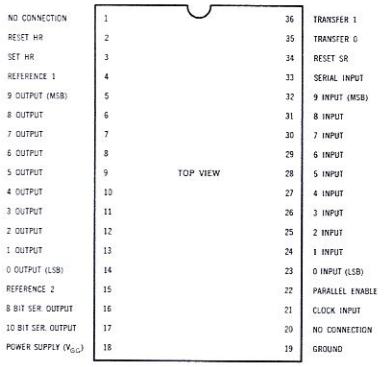


ORDER PART NO. A6H375014X

BLOCK DIAGRAM



PIN CONFIGURATION



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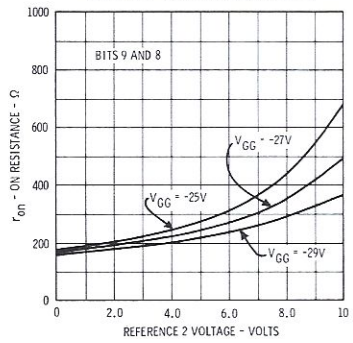
ELECTRICAL CHARACTERISTICS $V_{GG} = -27 \pm 2.0$ Volts, $R_L = 10\ M\Omega$, $C_L = 10$ pF (unless otherwise specified)

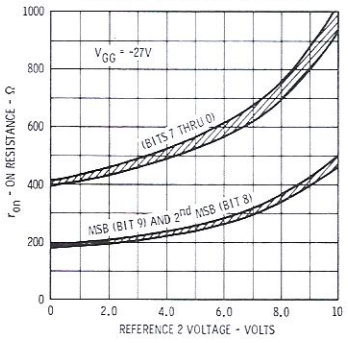
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Logic Inputs					
	"0"	0		−2.0	Volts	
	"1"	−9.0		−30	Volts	
	Logic Outputs					
	"0"	0		−1.0	Volts	
	"1"	−10		−30	Volts	
	Clock					
	Amplitude	−9.0		−30	Volts	
	Width	1.0		10	μs	
f_{max}	Frequency					
	Serial	DC		250	kHz	
	Parallel	DC		500	kHz	
r_{on}	MOS Switches					
	"9"	150	250	500	ohms	$V_{REF} = -5.0$ V
	"8"	150	250	500	ohms	$V_{GG} = -27$ V
	"7" thru "0"	325	550	1000	ohms	
Δr_{on}	Switch Mismatch					
	"9"		70	150	ohms	$V_{REF_2} = -5.0$ V
	"8"		70	150	ohms	$V_{REF_1} = 0$ V
	"7" thru "0"		120	250	ohms	
t_{df}	Serial Delay,		0.6		μs	
t_f	rise and fall		0.2		μs	
t_{dr}	times		0.5		μs	
t_r			0.5		μs	
t_{df}	Parallel Delay,		0.55		μs	
t_f	rise and fall		0.35		μs	
t_{dr}	times		0.4		μs	
t_r			0.3		μs	
C_{in}	Data and Control Input Capacitance		7.0		pF	
I_{max}	Power Supply Current Drain		4.5	7.0	mA	$V_{GG} = -27$ V
P_{max}	Power Dissipation		120	190	mW	$V_{GG} = -27$ V
	Temperature Coefficient of Switches		0.3		%/°C	
	Temperature Coefficient Tracking		0.03		%/°C	
I_{LX}	Input Leakage Current			5.0	μA	$V_{in} = -20$ V
t_{dd}	Data Delay Time	250			ns	

TYPICAL ELECTRICAL CHARACTERISTICS

ON RESISTANCE VERSUS POWER SUPPLY VOLTAGE (V_{GG}) OUTPUT VOLTAGE (REF. 2)

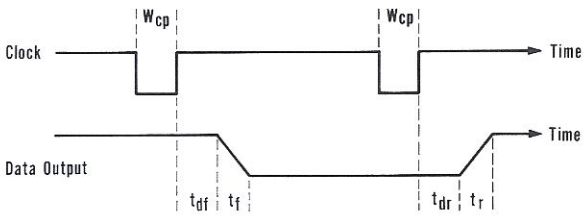


ON RESISTANCE VERSUS OUTPUT VOLTAGE (REF. 2)

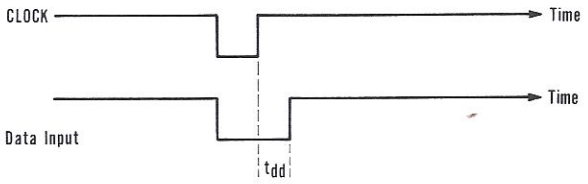


TIMING DIAGRAM

OUTPUT DELAY, RISE AND FALL TIMES

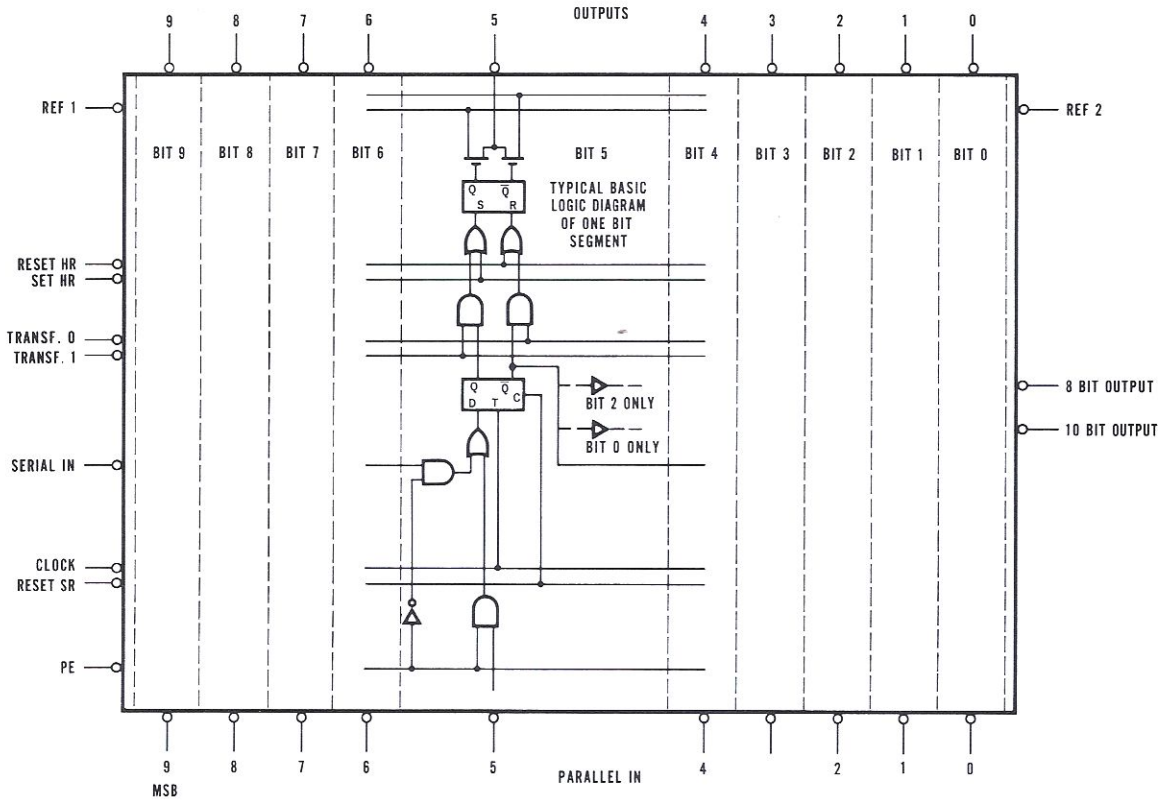


DATA BIT TIMING

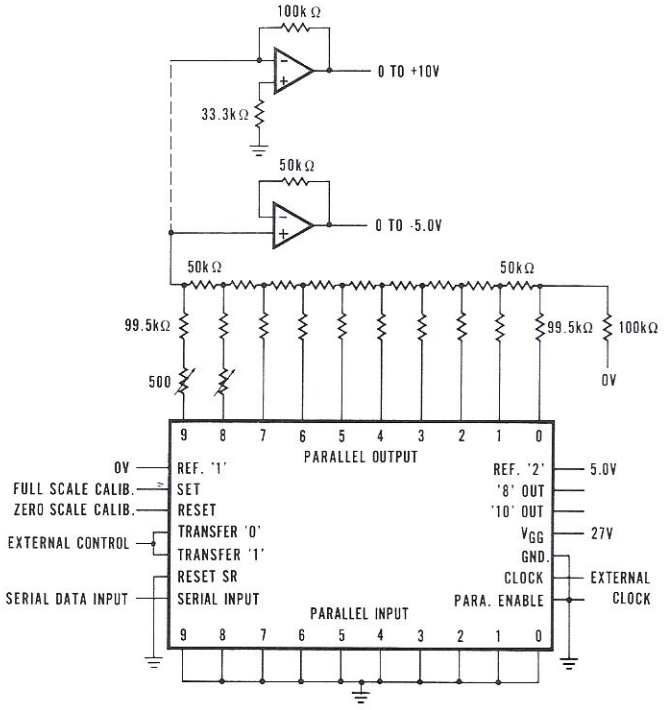


TIMING DIAGRAMS

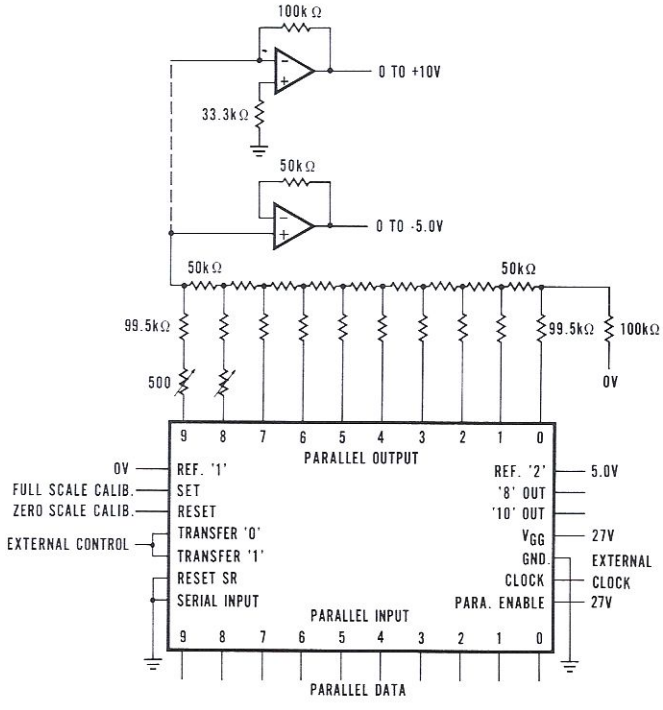
LOGIC DIAGRAM



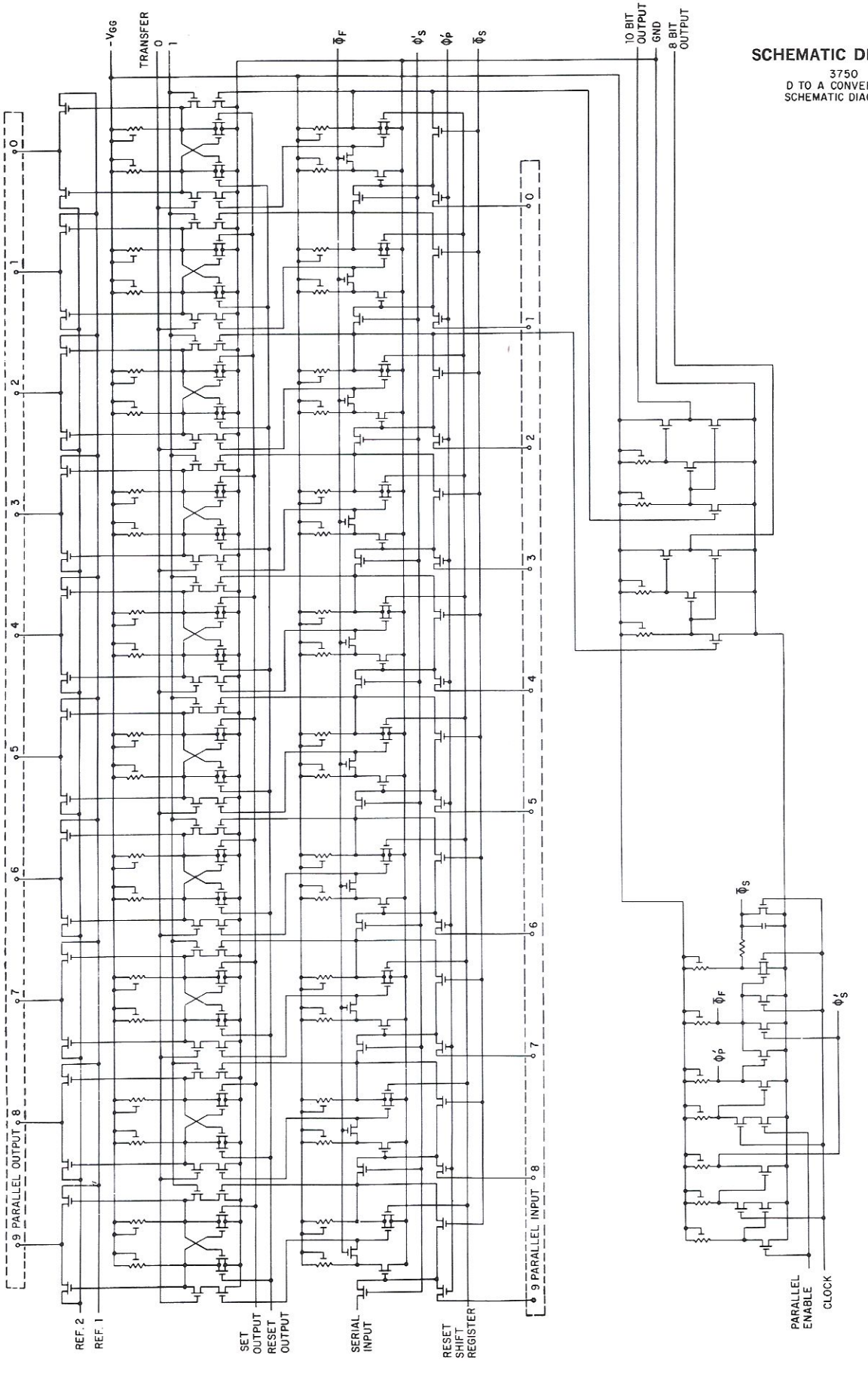
SERIAL OPERATION



PARALLEL OPERATION



FAIRCHILD MOS INTEGRATED CIRCUIT 3750



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